

Low Cost, Low Rate FPGA for 1-4 Mbps Applications

Definitions:

ACM	: Adaptive Coding and Modulation
A/Ds	: Analog to Digital Converters
ASIC	: Application Specific Integrated Circuit
D/As	: Digital to Analog Converters
FEC	: Forward Error Correction
FPGA	: Field Programmable Gate Array
LDPC	: Low Density Parity Check
QPSK	: Quaternary Phase Shift Keyed Modulation
QAM	: Quadrature Amplitude Modulation
RF	: Radio Frequency
Mbps	: Megabits per second
Msymb/sec	: Megasymbols per second
SoC	: System on a Chip

Description:

Wideband has previously developed a low cost low data rate modem and FEC core for oil and gas logging applications. The actual design of such a modem is somewhat more complex than the ASIC core we developed that operates up to 320 Mbps, however, such a design results in an extremely compact design that may be fielded in a modern Xilinx or Altera FPGA. This modem will operate up to a 0.5 Msymb/sec rate supporting QPSK through 256QAM and therefore data rates from 1 Mbps through 4 Mbps.

Through the reuse of multipliers, memory based delay elements, and other design techniques, the 1 Mbps core (0.5 Msymb at QPSK) is hosted in the FPGA. With the addition of low cost A/Ds and D/As and an engineered link only requiring a Reed Solomon FEC, an extremely low cost system may be fielded quickly. This FPGA system can be easily converted to an even lower cost, highly integrated SoC, once higher volume is required and the initial field tests are complete. This modem and network interface components will require less than 2 watts to operate.

Once this low rate core is placed into an ASIC part, it would be possible to incorporate the ACM, LDPC and Phase Noise immune upgrades during the high volume phase. The ACM and LDPC would facilitate longer links at the same data rates if required. The Phase Noise immune upgrades would permit lower RF equipment section costs.

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